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Solution for First Term Exanimation (2009-2010)

Q1): A) Fill in the blanks.

1) Flip-Flop is a _____memory_____ element.

2) The cascade of divide-by 5 counter followed by divide-by 2 counter is in state 0000. When a clock pulse is applied its state will be _____0010_____. Assume negative edge triggered circuits.

3) The speed of an asynchronous counter is _____less_____ than that of a synchronous counter.

4) A _____universal_____ shift register can be used for SISO, SIPO, PISO, and PIPO of data.

5) In an S-R Flip-Flop S=R=1 _____is not_____ permitted.

B) Choose the correct answer.

1) With a pulse-triggered flip-flop, the clock is applied directly to the _____master_____ latch, while the complement of the clock is applied to the _____slave_____ latch.

a. SET, RESET b. SET, master **c. master, slave** d. RESET, slave

2) What is another name for a flip-flop circuit?

a. Astable multivibrator b. Monostable multivibrator

c. Bistable multivibrator d. Tristable multivibrator

3) Which two multivibrator types require trigger input?

a. Astable and monostable **b. Monostable and bistable**

c. Bistable and astable d. Both a. and c. are true

4) The output pulse width of a 555 timer is determined by the externally connected _____Input resistor_____ and _____capacitor_____.

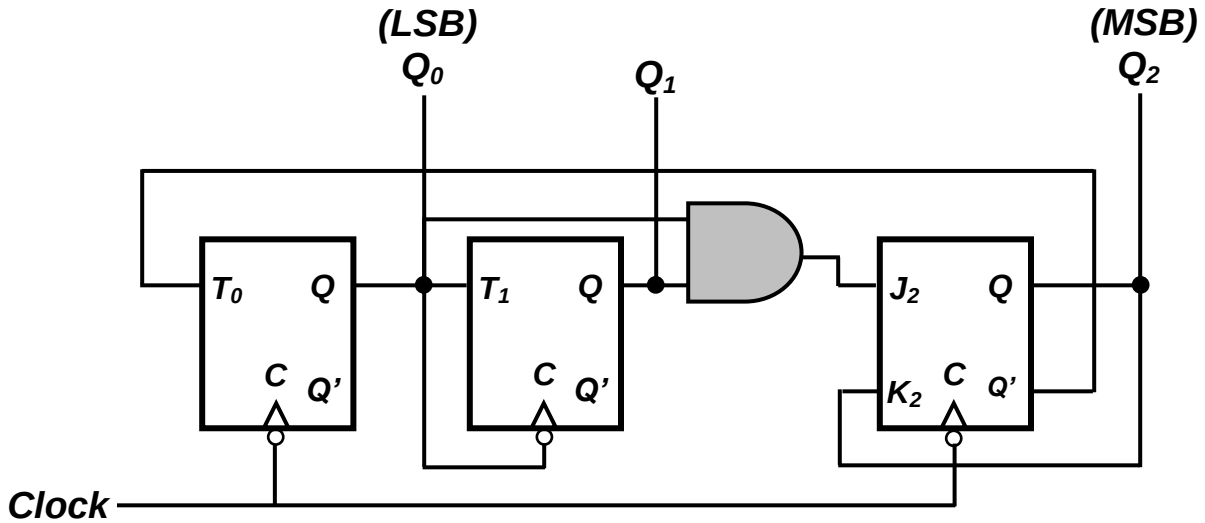
a. power supply, resistor b. load resistance, capacitor

c. capacitor, load resistor **d. input resistor, capacitor**

5) An eight-bit binary ripple UP counter with a modulus of 256 is holding the count 01111111. What will be the count after 135 clock pulses be?

a. 00001111 b. 00011010 c. 00000110 d. 00001100

Q2): Analysis the circuit shown in figure below:

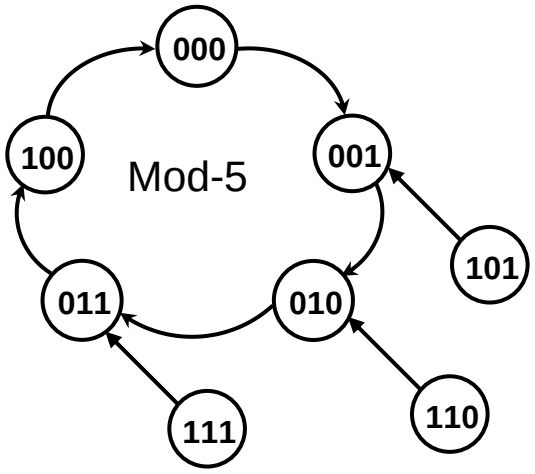


Solution: The counter input is: $J_2 = Q_1.Q_0.\ K_2 = Q_2.\ \ T_1 = Q_0.\ T_0 = Q'_2.$

The *present state – present input – next state* table will be as follows:

Present State			Present Input				Next State		
Q_2	Q_1	Q_0	J_2	K_2	T_1	T_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	1	0	0	1
0	0	1	0	0	1	1	0	1	0
0	1	0	0	0	0	1	0	1	1
0	1	1	1	0	1	1	1	0	0
1	0	0	0	1	0	0	0	0	0
1	0	1	0	1	1	0	0	0	1
1	1	0	0	1	0	0	0	1	0
1	1	1	1	1	1	0	0	1	1

The state transition diagram will be as shown below:



Then the counter is:

- Asynchronous counter.
- 3-bit counter.
- MOD-5.
- Divided by (5).
- Up Counter.
- Not self-starting.

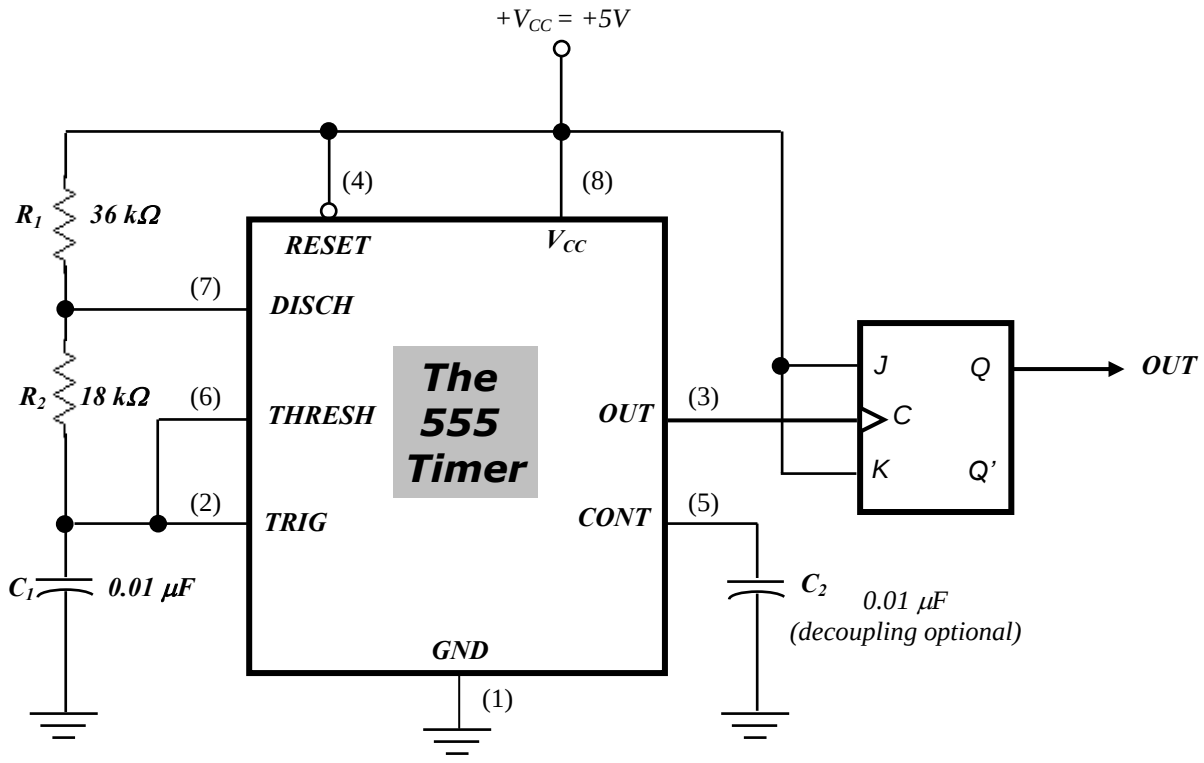
Q3: Figure below shows a typical clock-oscillator circuit using a (***555 timer***) and a (***J-K flip-flop***). Perform the following:

a) Calculate the output frequency from the ***555 timer***.

b) Determine the ***HIGH*** time and ***LOW*** time of the ***555 timer's output***.

c) Determine the output frequency from ***J-K flip-flop***.

d) Sketch the ***555 timer output*** and the ***Q output*** in time relation.



Solution:

a) $$f = \frac{1.44}{(R_A + 2R_2) \times C} \approx 2\ kHz.$$

b) $$t_{ON} = 0.7 \times C \times (R_1 + R_2) \approx 378\ \mu sec.$$

$$t_{OFF} = 0.7 \times C \times R_2 \approx 126\ \mu sec.$$

c) Since the J & K inputs of the flip-flop are normally tied ***HIGH***, the output will toggle and therefore divide the input frequency by two. Since we know that the 555 timer's output is (2 kHz), the J-K flip-flop's output will be (2 kHz ÷2 = 1 kHz).

d) The sketch will be as shown below: