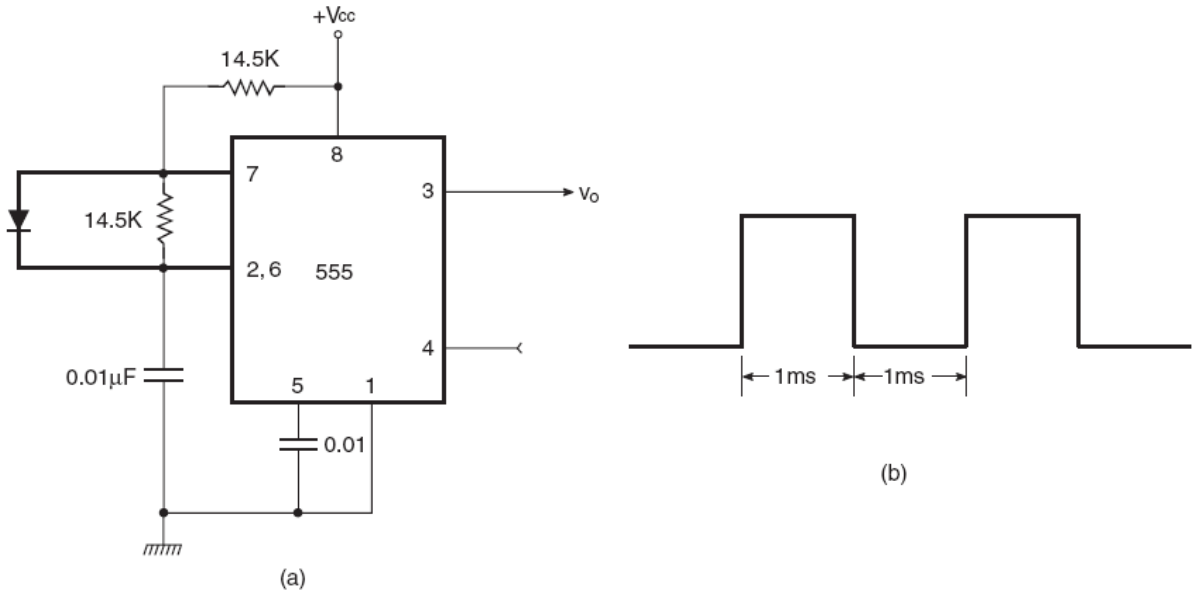
The Solution of the First Term Examination (2008-2009)

Q1): The pulsed waveform of Fig. (b) is applied to the ***RESET*** terminal of the astable multivibrator circuit of Fig. (a). *Draw the output waveform.*



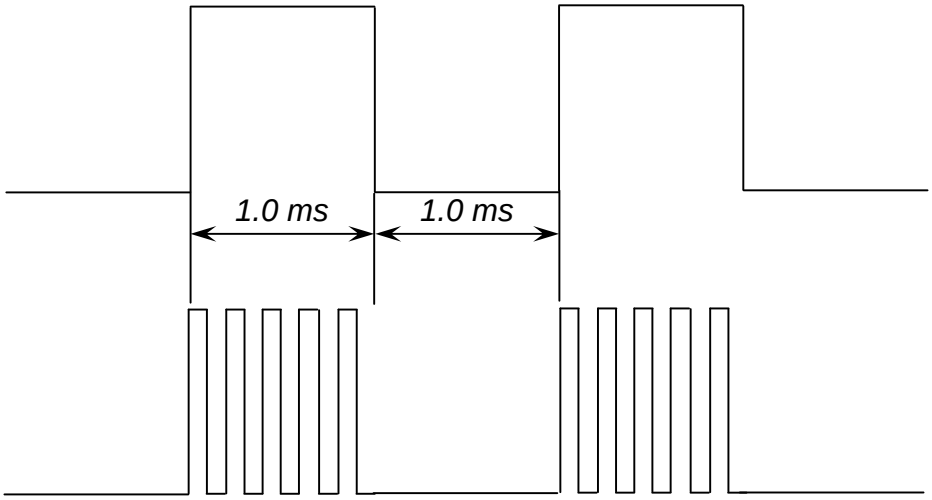
Solution:

The circuit shown in Fig. (a) is an astable multivibrator with a 500 Hz symmetrical waveform applied to its ***RESET*** terminal. The ***RESET*** terminal is alternately ***HIGH*** and ***LOW*** for *1.0 ms*. When the ***RESET*** input is ***LOW***, the output is forced to the ***LOW*** state. When the ***RESET*** input is ***HIGH***, an astable waveform appears at the output. The ***HIGH*** and ***LOW*** time periods of the astable multivibrator are determined as follows:

HIGH time = $0.69\times14.5\times10^{3}\times0.01\times10^{-6}$ = 0.1ms.

LOW time = $0.69\times14.5\times10^{3}\times0.01\times10^{-6}$ = 0.1ms.

The astable output is thus a *5 kHz* symmetrical waveform. Every time the *RESET* terminal goes to *HIGH* for *1.0 ms*, five cycles of *5 kHz* waveform appear at the output. Figure below shows the output waveform appearing at terminal 3 of the timer IC.



Q2): Design a ***3-bit up/down*** synchronous counter using ***T flip-flops***. It should include a control input called $Up/\overline{Down}$. If $Up/\overline{Down} = 0$, then the circuit should behave as a *down-counter*. If $Up/\overline{Down} = 1$, then the circuit should behave as an *up-counter*.

Solution:

The *present state – present input – next state* table will be as follows:

No.	Present State			U/D	Next State			Present Input		
	Q_C	Q_B	Q_A	C	Q_C	Q_B	Q_A	T_C	T_B	T_A
0	0	0	0	0=D	*1*	*1*	*1*	1	1	1
1	0	0	0	1=U	*0*	*0*	*1*	0	0	1
2	0	0	1	0	*0*	*0*	*0*	0	0	1
3	0	0	1	1	*0*	*1*	*0*	0	1	1
4	0	1	0	0	*0*	*0*	*1*	0	1	1
5	0	1	0	1	*0*	*1*	*1*	0	0	1
6	0	1	1	0	*0*	*1*	*0*	0	0	1
7	0	1	1	1	*1*	*0*	*0*	1	1	1
8	1	0	0	0	*0*	*1*	*1*	1	1	1
9	1	0	0	1	*1*	*0*	*1*	0	0	1
10	1	0	1	0	*1*	*0*	*0*	0	0	1
11	1	0	1	1	*1*	*1*	*0*	0	1	1
12	1	1	0	0	*1*	*0*	*1*	0	1	1
13	1	1	0	1	*1*	*1*	*1*	0	0	1
14	1	1	1	0	*1*	*1*	*0*	0	0	1
15	1	1	1	1	*0*	*0*	*0*	1	1	1

The K-map will be as follows:

T_C

$Q_C Q_B$ \ $Q_A C$	00	01	11	10
00	1			
01			1	
11			1	
10	1			

T_B

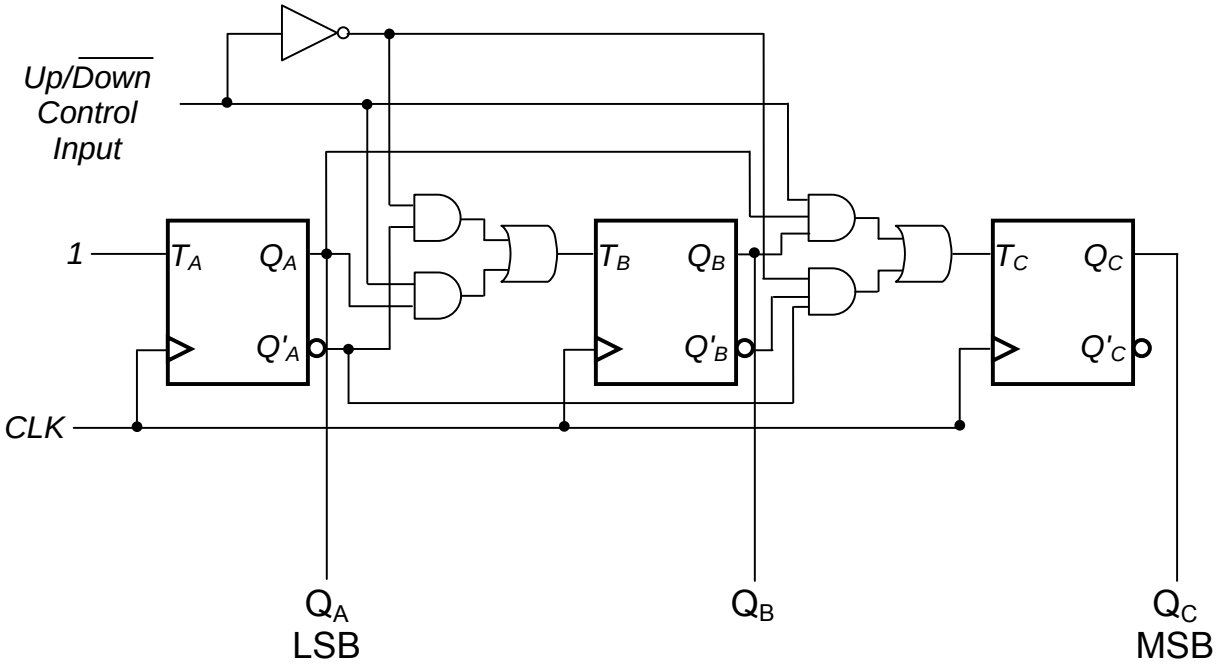
$Q_C Q_B$ \ $Q_A C$	00	01	11	10
00	1		1	
01	1		1	
11	1		1	
10	1		1	

T_A

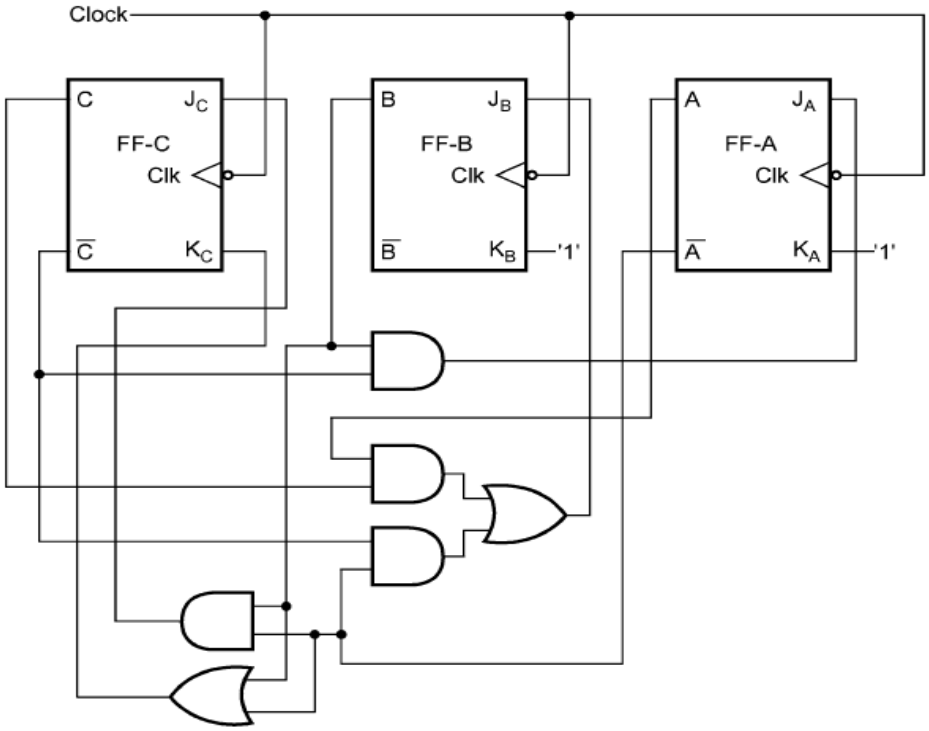
$Q_C Q_B$ \ $Q_A C$	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$T_C = Q`_B.Q`_A.C` + Q_B.Q_A.C.$ $T_B = Q`_A.C` + Q_A.C.$ $T_A = 1.$

The circuit diagram of the counter will be as shown below:



Q3): Analyze the counter shown in figure below.



Solution:

From figure above we have:

J_A=B. C`. K_A=1.

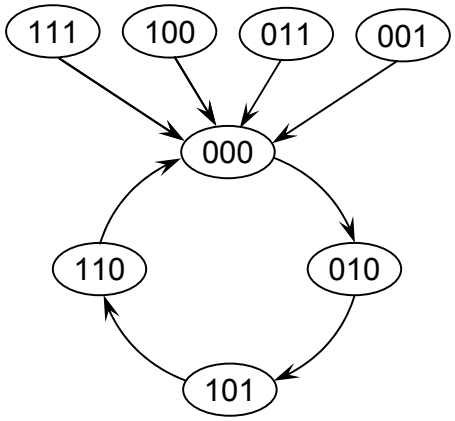
J_B=A.C + A`.C`. K_B=1.

J_C=A`. B. $K_C$=A`+ B.

The *present state – present input – next state* table will be as follows:

No.	Present State			Present Input						Next State			State
	C	B	A	J_C	K_C	J_B	K_B	J_A	K_A	C	B	A	
0	0	0	0	*0*	*1*	*1*	*1*	*0*	*1*	0	1	0	2
2	0	1	0	*1*	*1*	*1*	*1*	*1*	*1*	1	0	1	5
5	1	0	1	*0*	*0*	*1*	*1*	*0*	*1*	1	1	0	6
6	1	1	0	*1*	*1*	*0*	*1*	*0*	*1*	0	0	0	0
1	0	0	1	*0*	*0*	*0*	*1*	*0*	*1*	0	0	0	0
3	0	1	1	*0*	*1*	*0*	*1*	*1*	*1*	0	0	0	0
4	1	0	0	*0*	*1*	*0*	*1*	*0*	*1*	0	0	0	0
7	1	1	1	*0*	*1*	*1*	*1*	*0*	*1*	0	0	0	0

The state transition diagram will be as follows:



Then the counter classification is summarized here:

- MOD 4 (0, 2, 5, 6).
- Divided by 4.
- Synchronous.
- Three-bit.
- Negative edge-triggered.
- Binary up counter.
- Self-starting counter.