INTEGRATED CIRCUIT COUNTERS

Integrated circuit counters are available for counter applications that require serial up or down count sequences. The IC counters available are 4-bit binary or decade counters that can be cascaded together for applications requiring more than four output stages. The IC counters have asynchronous inputs that allow the flexibility of presetting the counter to an initial start value other than zero or resetting the counter back to zero at any instant of time. The 74LS193 and 74LS90 are two IC counters that are used in examples throughout this chapter.

The 74LS193 Four-Bit Binary Counter

The 74LS193 is a 4-bit synchronous, positive edge-triggered, binary counter capable of counting up or down. It has two asynchronous inputs for presetting and clearing the counter.

The 74193 is a programmable counter to allow either up or down counting and complete control over the count modulus through the use of the asynchronous inputs. Two separate clock inputs are used to control up or down counting.

The counter has a maximum MOD-16 count sequence that can be shortened to any modulus less than 16 by using the asynchronous control inputs. The clear input resets all count stages back to zero. The preset input sets the counter stages to any 4-bit binary number loaded on the parallel inputs of the 74LS193.

The counter can be easily cascaded while counting up or down through the carry output and borrow output to lengthen the modulus and to provide additional counter output stages.

An example of using the asynchronous inputs on the 74LS193 is shown in Example (15).

EXAMPLE (15): The 74LS193 Programmable Counter

Problem: Design a MOD-4 counter that produces the count sequence: 0, 1, 13, 14.

Solution: The count sequence is an up count that skips states 2 through 12 and 15. This count sequence can be achieved by forcing the counter to **load** the value 13

instead of the value 2, and by clearing the counter after the count state 14, as shown in Table (8).

Note that the counts 0 0 10 and 1 1 1 1 do not appear as output states. They are very narrow "spikes" in the output that are decoded by additional logic gates to load and clear the 74LS193 counter through the asynchronous load and clear inputs.

Table (8): Example (14) Count Sequence.

Count Output				Count Operations
QD	QC	QB	QA	
0	*0*	*0*	*0*	*Up Counting*
0	0	0	1	
0	*0*	*1*	*0*	*Decode 0 0 1 0 and load 1 1 0 1*
1	1	1	0	
1	*1*	*1*	*1*	*Decode 1 1 1 1 and Clear*

The asynchronous clear input on the 74193 is an active-HIGH logic input. Therefore, the output count states that represent the value *1 1 1 1* can be decoded with an AND gate, and the AND gate is input into the clear input. The asynchronous load input is an active-LOW logic input. The output count state *0 0 1 0* should be decoded with a NAND gate, and the output of the NAND gate is input to the load control. The parallel load inputs of the counter should be tied to the constant logic levels of *1 1 0 1* to load the value of 13 when dictated by the NAND gate decoder. The final circuit for Example (15) is shown in Figure (24). The state transition diagram also shown in Figure (24), indicates how all possible states will reach the count sequence.

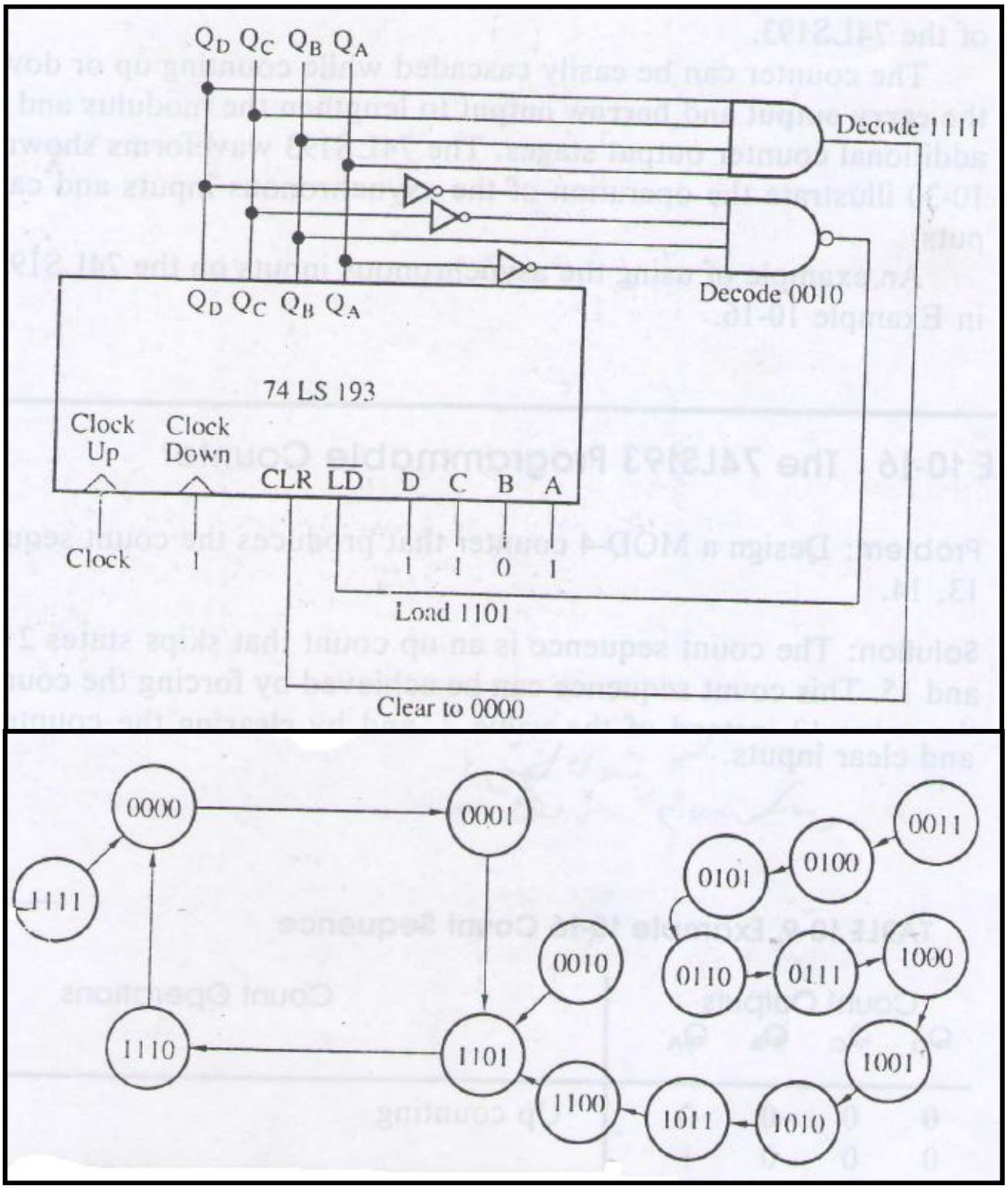

Figure (24): 74LS193 Example (15) Circuit.

The 74LS90 Decade Counter

The 74LS90 is a 4-bit asynchronous, negative edge-triggered decade counter with asynchronous clear and present inputs for programmable counter applications.

The 74LS90 counts only in an ascending sequence. The IC actually consists of two separate counters that can be configured for three different modes of operation. The two internal counters are a MOD-2 counter and a MOD-5 counter, providing a total of four output stages.

Mode 1: The MOD-2 and MOD-5 counters operate separately with individual clock inputs. The MOD-2 counter toggles from a logic HIGH to a logic LOW state on each clock pulse. The MOD-5 counter produces a 3-bit count sequence from 0 to 4. Figure (25) shows the 74LS90 in this configuration, along with the resulting waveforms and state transition diagrams.

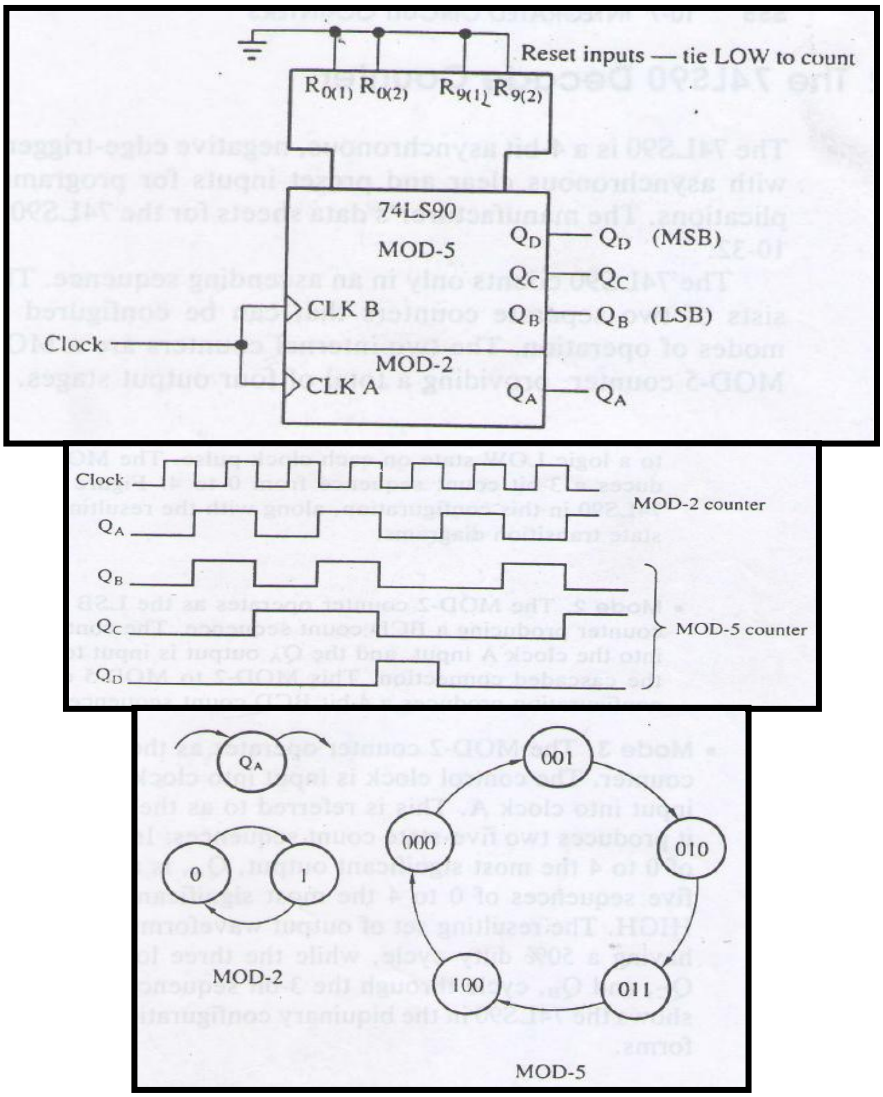

Figure (25): 74LS90 MOD-2 and MOD-5 Counters.

Mode 2: The MOD-2 counter operates as the LSB of a 4-bit decade counter producing a BCD count sequence. The control clock is input into the clock A input, and the Q_A output is input to clock B to form the cascaded connection. This MOD-2 to MOD-5 cascaded counter configuration produces a 4-bit BCD count sequence of 0 to 9. Figure (26) shows the 74LS90 connected in this configuration and the output waveforms.

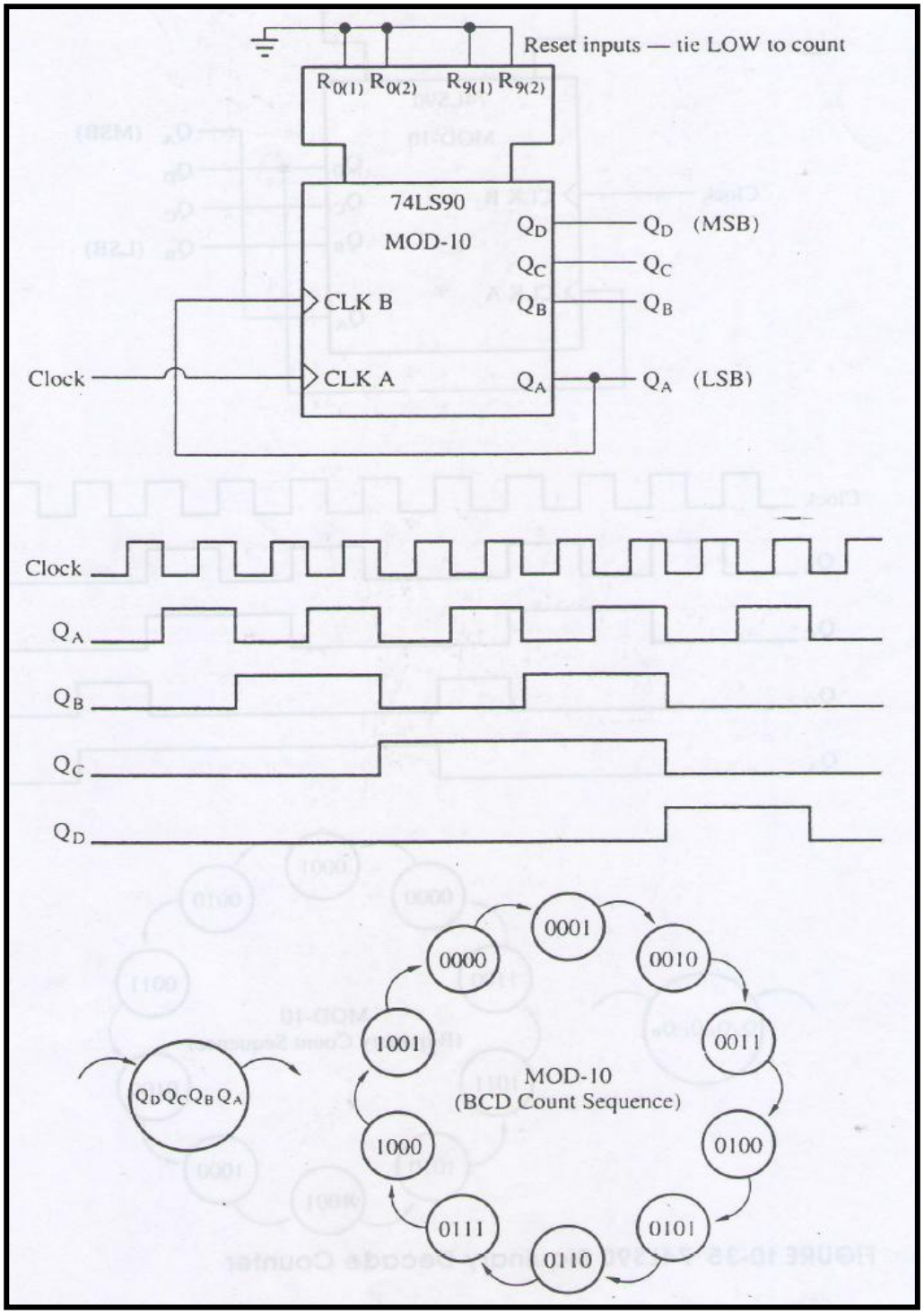

Figure (26): 74LS90 Decade Binary Code Decimal Counter.

Mode 3: The MOD-2 counter operates as the MSB of a 4-bit decade counter. The control clock is input into clock B and the Q_D output is input into clock A. This is referred to as the ***biquinary counter*** since it produces two five-state count sequences: In the first five sequences of 0 to 4 the most significant output, Q_A, is a logic LOW; in the last five sequences of 0 to 4 the most significant output, Q_A, is logic HIGH. The resulting set of output waveforms are with the Q_A output having a 50% duty cycle, while the three lower order outputs, Q_D, Q_c, and Q_B, cycle through the 3-bit sequence of 0 to 4. Figure (27) shows the 74LS90 in the *biquinary* configuration with the output wave-forms.

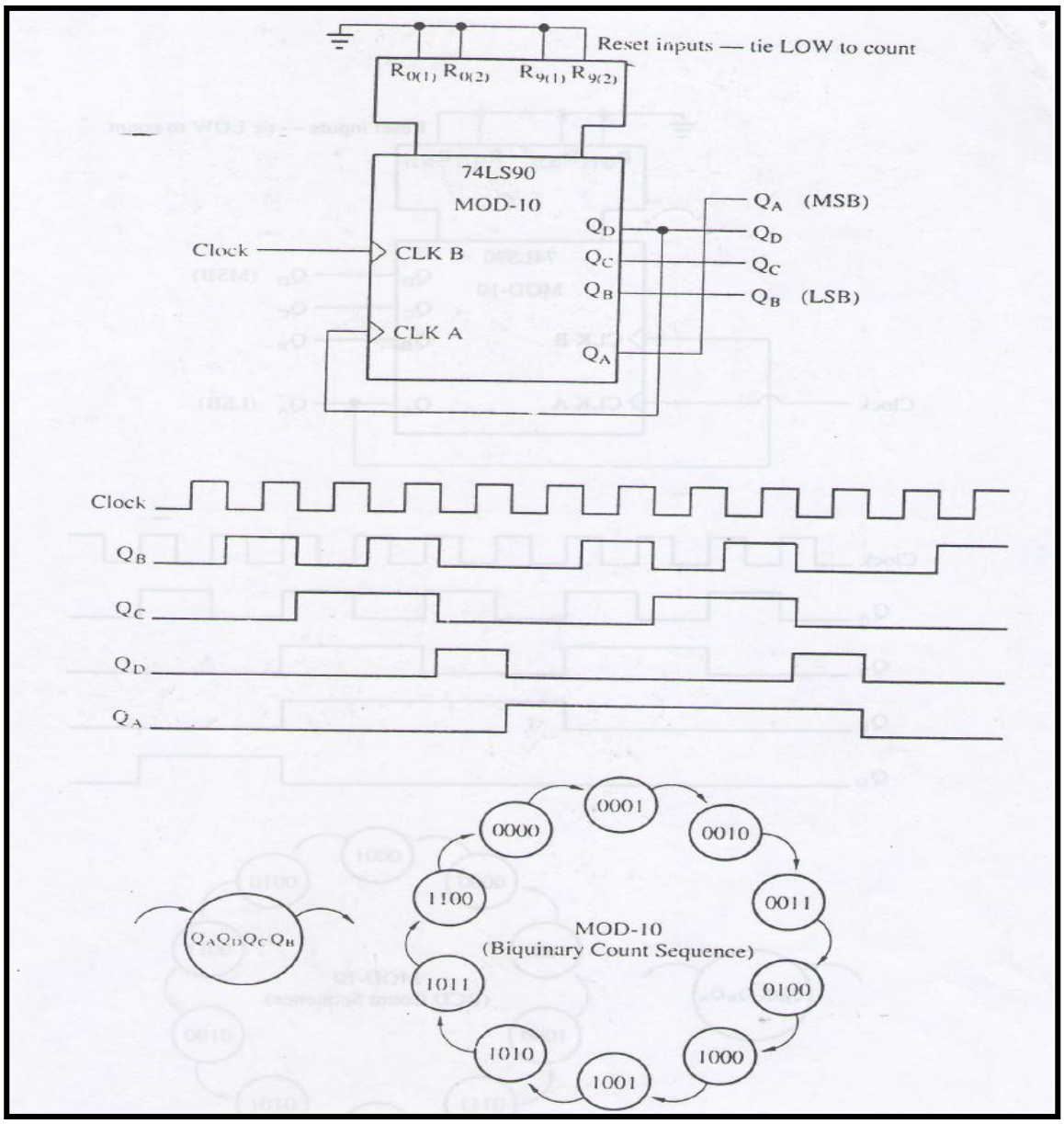

Figure (27): 74LS90 Biquinary Decade Counter.

EXAMPLE (16): The 74LS90 Counter Application

Problem: Design a MOD-6 BCD counter using the 74LS90.

Solution: The 74LS90 can only count up and can only be reset to zero or preset to 9. To design a MOD-6 BCD counter, the 74LS90 must be configured with Q_A as the LSB (mode 2), and the seventh count state, *0110*, must be decoded to reset the counter to *0000*. The count sequence and the 74LS90 operation are shown in Table (9).

Table (9): 74LS90 MOD-6 BCD Counter Operation.

Counter Outputs				Counter Operation
QD	QC	QB	QA	
0	*0*	*0*	*0*	*Up Counting*
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	*1*	*1*	*0*	*Decode 0110 and reset*

Note that the *0 1 1 0* output state is seep only as a spike in the output waveforms. As soon as the *0 1 1 0* state is reached, it is decoded using additional logic gates and the counter resets to *0 0 0 0*. The circuit configuration to perform this count sequence is shown in Figure (28).

Integrated Circuit Counter Selection

Numerous IC counters are available as transistor-transistor logic (TTL) and complementary metal-oxide semiconductor (CMOS) logic devices. Selection of a counter circuit for a particular application should be based on matching the requirements of the application to the capabilities of the counter Key parameters that should be checked include counter modulus, maximum clock frequency, clock pulse requirements, cascade inputs and outputs count enable inputs, and asynchronous

preset and clear inputs Table (10) lists several common TTL counter ICs available today.

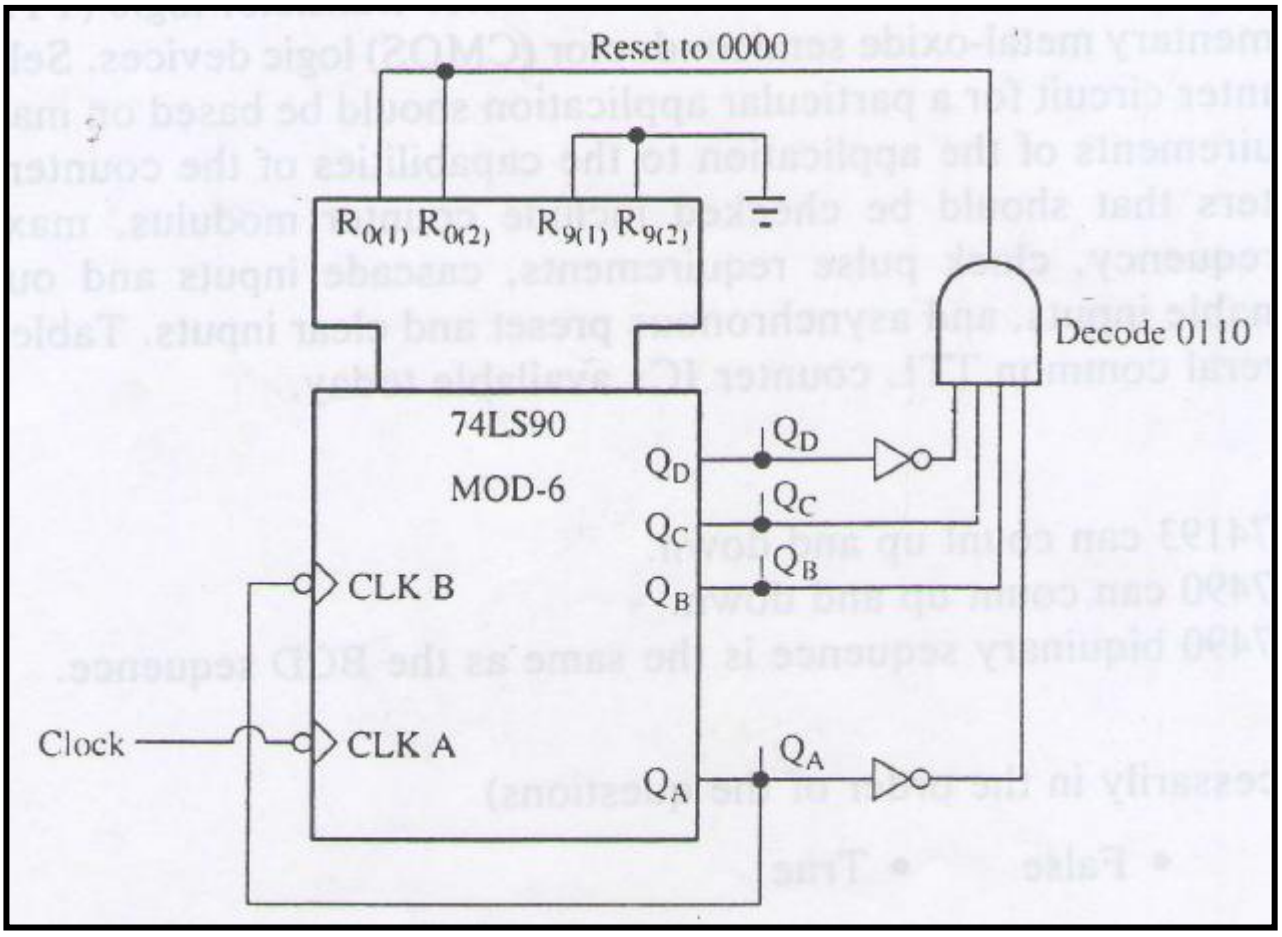

Figure (28): 74LS90 Example (16) Counter Circuit.

Table (10): Integrated Circuit Counters.

Synchronous Counter				
74LS160	Decade	Up	Asynch., clear	32 MHz
74LS161	Binary	Up	Asynch., clear	32 MHz
74LS162	Decade	Up	Synch., clear	32 MHz
74LS163	Binary	Up	Synch., clear	32 MHz
74LS190	Decade	Up/Down	Asynch., load	25 MHz
74LS191	Binary	Up/Down	Asynch., load	25 MHz
74LS192	Decade	Up/Down	Load/Clear	32 MHz
74LS193	Binary	Up/Down	Load/Clear	32 MHz

Asynchronous Counter				
74LS90	Decade	Up	Load 9 or 0	32 MHz
74LS92	MOD 12	Up	Clear	32 MHz
74LS93	Binary	Up	Clear	32 MHz
74LS196	Decade	Up	Load/Clear	30 MHz
74LS390	Decade (equivalent to dual 74LS90)			25 MHz
74LS393	Binary (equivalent to dual 74LS93)			25 MHz

Section Self-Test

1. The 74193 can count up and down.
2. The 7490 can count up and down.
3. The 7490 biquinary sequence is the same as the BCD sequence.

ANSWERS: (Not necessarily in the order of the questions).

• False. • False. • True.