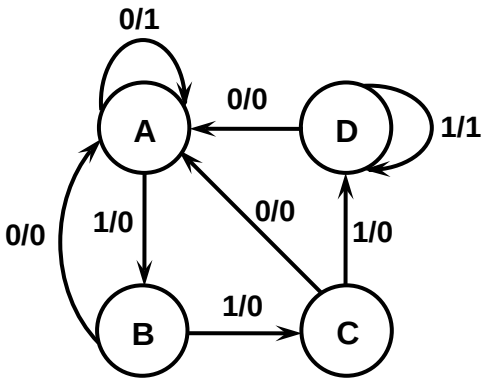
The Solution of First Term Examination (4th Class)
2010-2011

Q1) Use ***T-flip-flops*** to design a ***Mealy*** system that produces a *1* output if there have been ***four or more*** consecutive *1* inputs or ***two or more*** consecutive *0* inputs.

Solution:

We start with a state for which the last input is (0). From there, we need four consecutive (1's) to get a (1) output or another (0). Thus, on additional (0's), we loop back to state (A). On a (1), we go to (B); on a second (1), we go to (C); and on a third (1), we go to (D). In (D), additional (1's) produce a (1) output; (0's) return the system to state (A). The state diagram will be as follows:



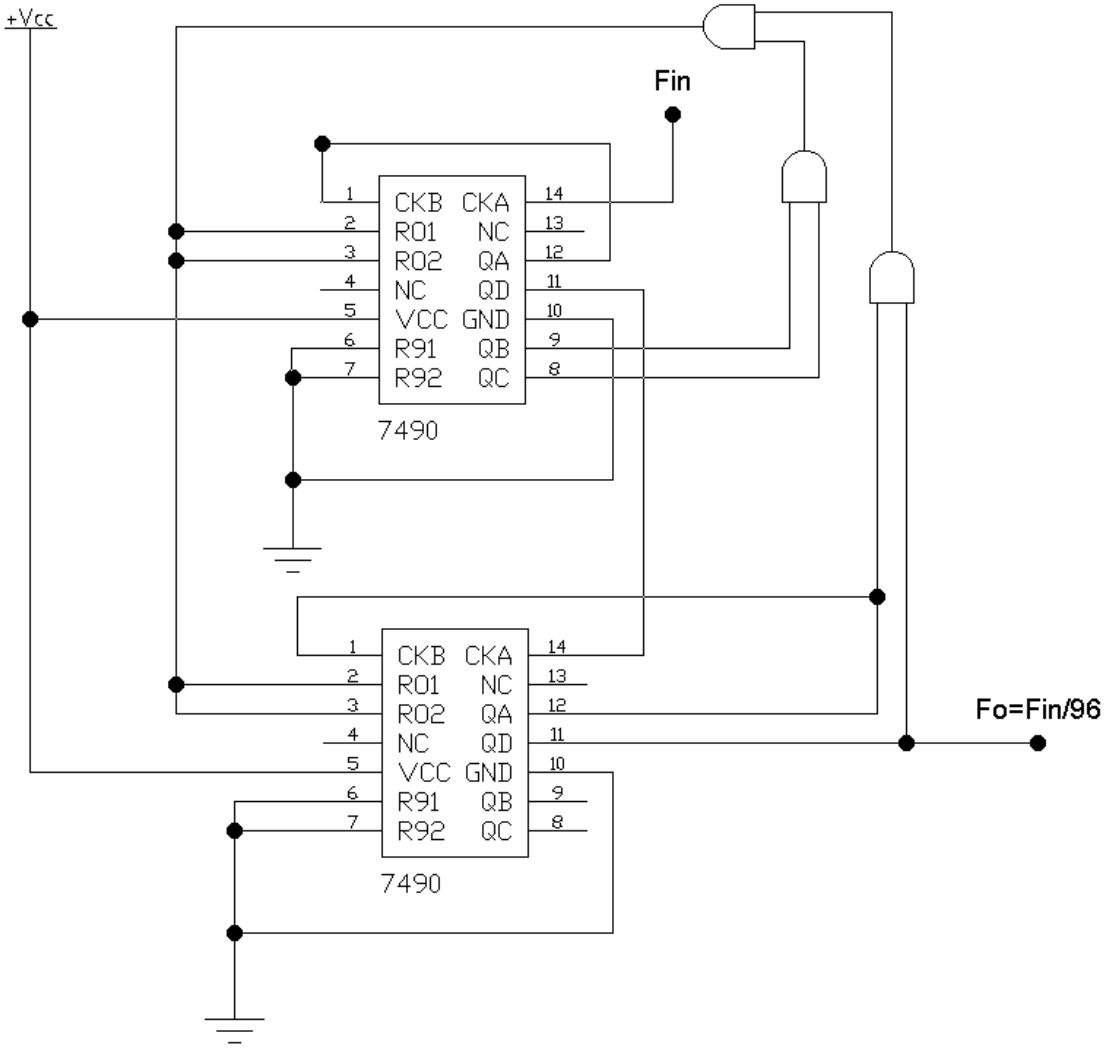
The state table will be as follows:

Present State	Next State		Output	
	X=0	X=1	X=0	X=1
A	A	B	1	0
B	A	C	0	0
C	A	D	0	0
D	A	D	0	1

Q2) Design a ***MOD-96*** asynchronous counter using minimum number of ***74LS90s*** ICs. Explain how the ***MOD-96*** circuit functions, based on the count sequence and decoding operations.

Solution:

The designed circuit of MOD-96 by using two ICs of ***74LS90s*** asynchronous counter as shown in figure below:



Q3) Table (1) gives the excitation table of a certain flip-flop having ***(X_1 & X_2)*** as its inputs. Draw the circuit excitation table of an ***MOD-5*** synchronous counter using this flip-flop for the count sequence ***(0, 1, 3, 5, 6, 0, ...)***. If the present state is an undesired one, it should transit to ***(6)*** on application of a clock pulse. Design the counter circuit using the flip-flop whose excitation circuit is given in Table (1).

Table (1)

Present state (Q_n)	Next state (Q_{n+1})	Inputs	
		X_1	X_2
0	0	0	0
0	1	0	1
1	0	1	X
1	1	X	1

Solution:

- The circuit excitation table is shown in Table (2).
- The number of flip-flops required is (3).
- X1(A) and X2(A) are the inputs of flip-flop (A), which is also the LSB flip-flop.
- X1(B) and X2(B) represent the inputs to flip-flop (B).
- X1(C) and X2(C) are the inputs to flip-flop (C), which is also the MSB flip-flop.
- The next step is to draw Karnaugh maps, one each for different inputs to the three flip-flops.
- Figures (1)(a) to (f) show the Karnaugh maps for X1(A), X2 (A), X1(B), X2(B), X1(C) and X2(C) respectively.
- The minimized expressions are as follows:

  X1(A) = A. X2(A) = A + B'C'.
  X1(B) = B. X2(B) = A + B + C.
  X1(C) = C. X2(C) = B + C.

- Figure (2) shows the circuit implementation.

Table (2)

Present state			Next state			Inputs					
C	*B*	*A*	*C*	*B*	*A*	$X_1(A)$	$X_2(A)$	$X_1(B)$	$X_2(B)$	$X_1(C)$	$X_2(C)$
0	0	0	0	0	1	0	1	0	0	0	0
0	0	1	0	1	1	X	1	0	1	0	0
0	1	0	1	1	0	0	0	X	1	0	1
0	1	1	1	0	1	X	1	1	X	0	1
1	0	0	1	1	0	0	0	0	1	X	1
1	0	1	1	1	0	1	X	0	1	X	1
1	1	0	0	0	0	0	0	1	X	1	X
1	1	1	1	1	0	1	X	X	1	X	1

X = don't care condition.

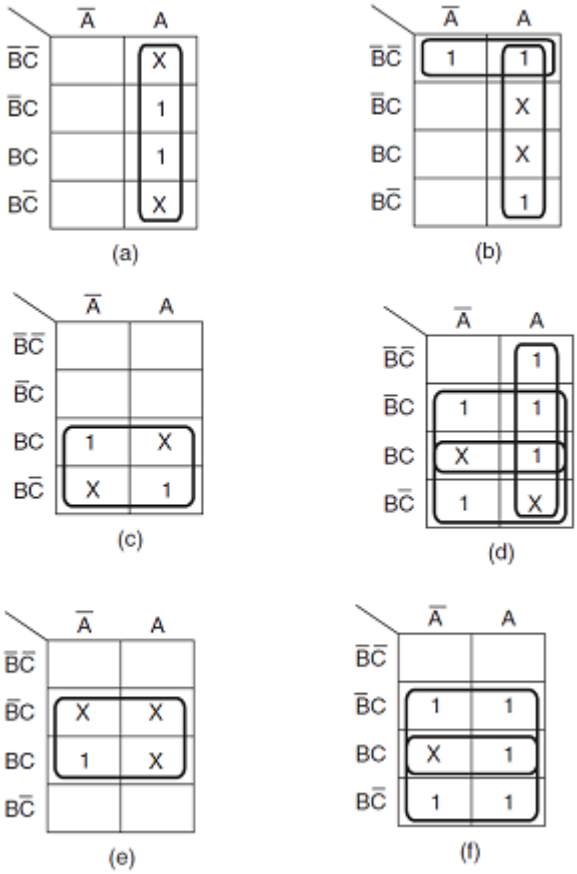


Figure (1): Karnaugh maps.

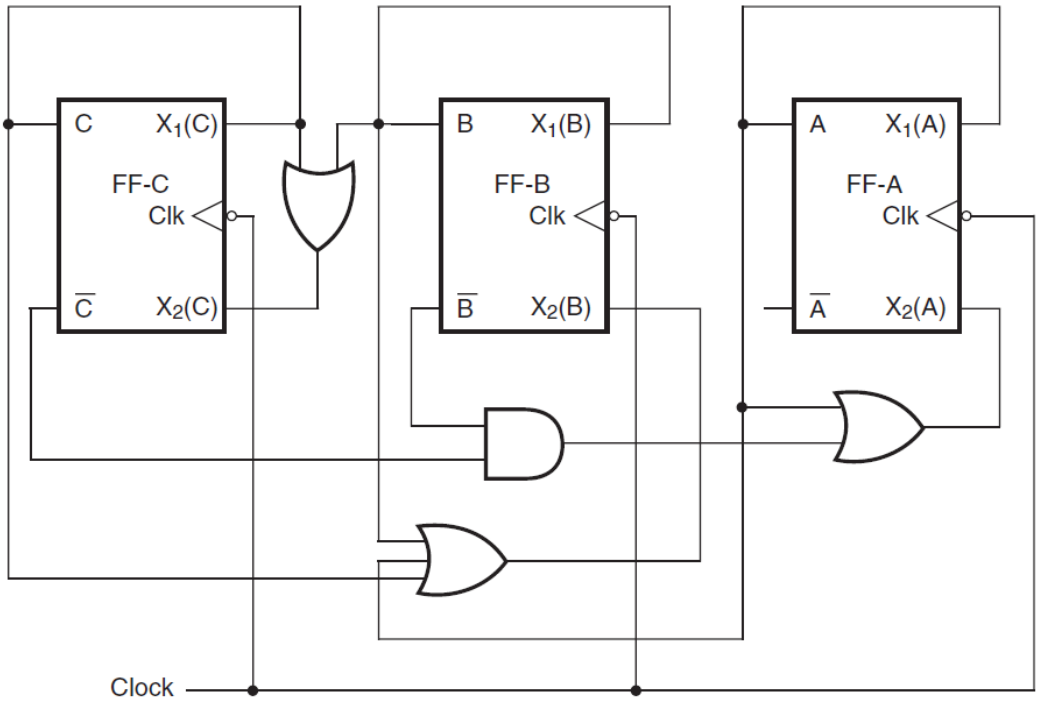


Figure (2): Counter circuit.