

Chapter 9

Integrated Circuit Fabrication

9.1: Category of Integration

SSI \rightarrow Small Scale integration

MBS \rightarrow Medium " "

LSI \rightarrow Large " "

VLSI \rightarrow Very large " "

< 10 gates per chip

10-100 " " "

100-1000 " " "

> 1000 " " "

chip:- Tiny piece of Semiconductor crystal which all components of an IC are constructed on it.

Monolithic IC:- IC Fabricated entirely on a single Silicon Crystal.

hybrid IC:- Contain one or more monolithic interconnected with external res. or capacitors.

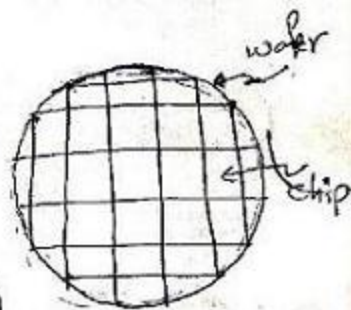
9.2 Monolithic IC Technology steps

IC Fabrication consists of ^{six or} ~~seven~~ independent steps.

9.2.1: Crystal Growth of wafer

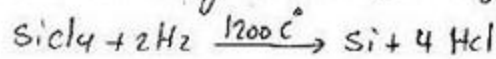
A single p-type crystal ingot of order (10 cm) in diameter & (50 cm) long is grown. By Cz (Technique), the ingot is subsequently sliced into round (wafers) approx.

(0.2-0.3 mm) in thickness that forms the substrate on which all integrated components will be fabricated. The ~~wafer~~ wafer is sawed into 100 to 10000 rectangular chips having sides of 1 to 10 mm.



9.2.2: Epitaxial Growth

It is used to grow a layer of single-crystal silicon as an extension of an existing crystal wafer. It is performed in a furnace called a reactor in which silicon wafer are heated to $900-1000^{\circ}\text{C}$. Current Technology uses the hydrogen reduction of gases SiH_4 or SiCl_4 as a source of silicon to be grown



An n-type epitaxial layer typically $(6-25)\mu\text{m}$ -thick is grown into a p-type substrate. n-type or p-type impurities such as phosphorus (PH_3) for n-type & ~~boron~~ diborane (B_2H_6) for p-type must be introduced in the SiCl_4 gas.

9.2.3: Oxidation

Silicon Technology has the ability to grow oxide layer on the silicon wafer surface. The silicon dioxide has the capability of being etched by hydrogen fluoride (HF) & the impurities used to dope the silicon do not penetrate the silicon dioxide. one method is to pass oxygen over the surface of silicon wafer at 1200°C & its thickness is about $0.02-2\mu\text{m}$. Fastest growth may be obtained by passing steam on the wafer



9.2.4 photolithography

It is used to select & remove regions of SiO_2 to form opening through which impurities may be diffused. It involves two operations:

9.2.4.1: Mask production:

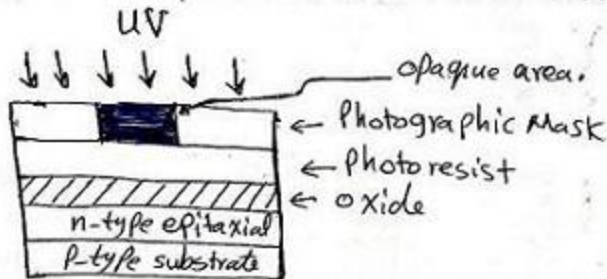
It involves complicated and expensive processes. After the cell layout has been determined, a large scale drawing is made showing the locations of openings to be etched in SiO_2 .

The drawing is magnified to scale 500:1, so several reduction stages are required (masking levels).

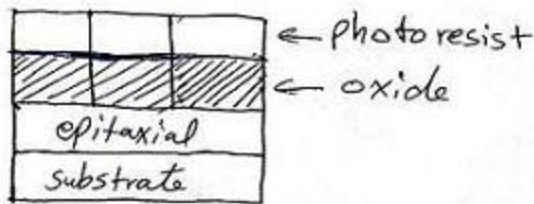
9.2.4.2. ∴ Photo-etching

It etches the ~~SiO₂~~ SiO_2 for cutting the windows for diffusion. Initially the slice is covered with thin film photoresist, & then the slice exposed to (Ultra Violet UV) light. The opaque area of the mask correspond to the area to be etched away, as in Fig(1)

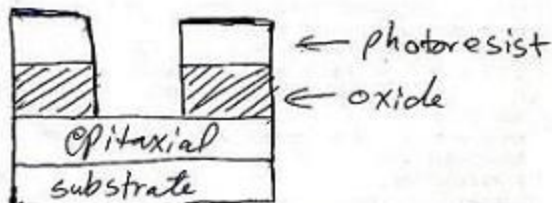
- (a) Exposure ^{the} photoresist to UV, so the transparent region will be polymerized.



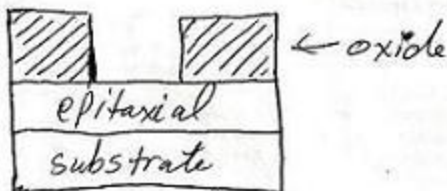
- (b) washing using trichloro ethylene



- (c) Etching by hydrofluoric acid (HF)



- (d) stripping of photoresist by chemical solvent (H_2SO_4).



9.2.5: Diffusion:-

It is used to diffuse impurities into the slice. the impurity concentration is performed in a diffusion furnace at a Temp. of about 1000°C over a 1-2 ~~one~~ hours. Impurities sources can be gases, liquids or solids. Gases impurities is more popular and generally the hydrides of Boron or Arsenic AsH_3 & Phosphorus PH_3 are the famous.

9.2.6: Ion Implantation

It is a second method of introducing impurities in a vacuum. A beam of ions are accelerated by energies between 30 - 200 KeV. The depth of penetration of these ions is determined by the accelerated energy and the beam current. It is used when a thin layer of doped silicon is required such as Emitter in BJT. This is performed in low Temp.

9.2.7: Metalization:-

It is used to form interconnections of component on chip. These are formed by the deposition of thin film layer of Aluminium & Gold over entire surface of chip. A mask is used to define the connection pattern between components and unwanted aluminum is removed.